Abstract of the Disclosure:

A memory cell configuration connects two trench capacitors to a bit line through a contact bit terminal. Trench capacitors are disposed in a regular grid. Word and bit lines are disposed in a mutually perpendicular crossover structure. An active region in which a selection transistor of an adjoining trench capacitor is introduced is disposed respectively between two trench capacitors of a row. Trench capacitors of two rows are laterally offset with respect to one another. Two active regions of adjacent rows are electrically connected to one another through a connecting line. Connected active regions form a common terminal region connected to a contact bit terminal, which is connected to a bit line. Bit lines are disposed between rows of trench capacitors and parallel thereto. By reducing the contact bit terminals, capacitances of the bit lines are reduced and interference signal transmission between word line and contact bit terminals is reduced.

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